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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,142	11/16/2001	James S. Dunn	BUR920000140US1	4751

7590 03/23/2005

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,142	DUNN ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-14 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,14* is/are allowed.

6)☒ Claim(s) *1-10,12,20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference character "168" (see page 7, second paragraph). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than obvne year prior to the date of application for patent in the United States.

3. Claims 1, 2, 7 thru 9, 12, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yagi et al. 4,038,680. Yagi discloses (see, for example, Fig. 7J) a PNP transistor (first semiconductor device) PNP Tr1, P type region (first subcollector) 78, NPN transistor (second semiconductor device) NPN Tr2, and N type region (second subcollector) 88. The N type region differs from P type region by impurity type. In column 10, lines 17-19, Yagi discloses the P type region 78 serving as a collector region for the PNP transistor. In column 10, lines 42-46, Yagi discloses the N type region 88 serving as a collector region for the NPN transistor. Yagi further discloses the sheet resistance being about 100 ohms/square. Regarding the limitation "to provide lateral ballasting effect", it has been held that a recitation with respect to the manner in

which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus **satisfying the claimed structural limitations**. Ex Parte Masham, 2 USPQ F. 2d 1647 (1987).

Regarding claims 8 and 9, see, for example, P type region (additional diffusion) 84.

4. Claims 1, 2, 6 thru 9, 12, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. 4,258,379. Watanabe discloses (see, for example, FIG. 8) a NPN transistor (first semiconductor device) 101, antimony buried layer (first subcollector) 21, IIL section (second semiconductor device) 201, and phosphorous buried layer (second subcollector) 22''. The phosphorous buried layer differs from the antimony buried layer by element. In column 7, lines 39-41, Watanabe discloses the sheet resistivity of the phosphorous buried layer being 50-100 ohms/square and the sheet resistivity of the antimony buried layer being 10-30 ohms/square.

Regarding claims 8 and 9, see, for example, N type layer (additional diffusion) 41'.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 thru 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. '379 as applied to claims 1, 2, 6-9, 12, and 21, and further in view of Yamaguchi 63-288055 JPO. Watanabe does not disclose said first subcollector comprising an arsenic impurity

and said second subcollector comprising an antimony impurity. However, Yamaguchi discloses (see, for example, figure 1) a bipolar transistor (first semiconductor device) 40 and an IIL transistor (second semiconductor device) 50. The bipolar transistor has a buried layer (first subcollector) 120 comprising antimony and the IIL transistor has a buried layer (second subcollector) 130 comprising arsenic. In the abstract, Yamaguchi discloses improved amplification factor and frequency characteristics without damaging the breakdown strength. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said first subcollector comprising an arsenic impurity and said second subcollector comprising an antimony impurity in order to improve amplification factor and frequency characteristics without damaging the breakdown strength.

Regarding claim 4, Watanabe does not disclose said first subcollector comprising an implant dose in the $1X10^{16}cm^{-2}$ range and said second subcollector comprising an implant dose in the $1X10^{15}$ cm^{-2} range. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use this range in order to improve the amplification factor and frequency characteristics between the first subcollector and the second subcollector, and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 5, the limitation "said second subcollector provides a higher resistance and a higher breakdown voltage than said subcollector" is an inherent limitation based on the structure wherein the first subcollector comprises arsenic impurity and the second subcollector comprises antimony impurity.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. '379 as applied to claims 1, 2, 6-9, 12, and 21, and further in view of Hebert et al. 6,365,447 B1. Watanabe does not disclose said first subcollector comprising having an edge defined by a deep trench. However, Hebert discloses (see, for example, FIG. 2) a semiconductor wafer comprising buried layers 14, 16 and a vertical trench isolation structures. The trench isolation structures define the edges of the buried layers and separate adjacent devices. The trench isolations provide side wall isolation for adjacent devices. See, for example, column 5, lines 25-28. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have an edge defined by a deep trench in order to provide side wall isolation between adjacent devices.

8. Claims 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. '379 as applied to claims 1, 2, 6-9, 12, and 21 above, and further in view of Washio et al. 4,694,321. Watanabe does not disclose said second subcollector having a different doping concentration. However, Washio discloses (see, for example, FIG. 2) a first bipolar transistor (first semiconductor device) 100 and an integrated injection logic (second semiconductor device) 200. The first bipolar transistor has a buried layer (first subcollector) 2 and the integrated injection logic has a buried layer (second subcollector) 22. In column 2, lines 33-40, Washio discloses the buried layer 22 having an impurity concentration greater than the buried layer 2 wherein the impurity concentration prevents the current from reaching the substrate and increasing the current gain. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to said second subcollector having a different

doping concentration in order to prevent current from reaching the substrate and increasing current gain.

Allowable Subject Matter

9. Claims 13, and 14 are allowed. The following is a statement of reasons for the indication of allowable subject matter: The references of record, either singularly or in combination, do not teach or suggest at least first and second bipolar transistors formed on a p-substrate, said first transistor comprising: a Sb subcollector; a n-epi collector; a SiGe polysilicon p-doped extrinsic base; a SiGe silicon single crystal intrinsic base; and said second transistor comprising: an As subcollector having a sheet resistance at 50-200 ohms/square; a n-epi collector; a SiGe polysilicon extrinsic base; and a SiGe single crystal extrinsic base.

Response to Arguments

10. Applicant's arguments with respect to claims 1-10, 12-14, and 20-22 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the applicant's argument on page 8, last paragraph that no subcollectors are referred to, and there does not appear to be any sheet resistance characteristic which would improve lateral ballasting of the transistor, this argument is not persuasive. In Fig. 7J and in column 10, lines 17-19, Yagi discloses the P type region (first subcollector) 78 serving as a collector region for the PNP transistor and in column 10, lines 42-46, Yagi discloses the N type region (second subcollector) 88 serving as a collector region for the NPN transistor. These regions clearly reside under ("sub" collector) the surface of the substrate. In column 10, lines

42-45, Yagi discloses the N type region 88 having a sheet resistance being about 100 ohms/square which is the sheet resistance characteristic (exceeding 50 ohms/square) disclosed in the applicant's claims.

Regarding the limitation "to provide lateral ballasting effect", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus **satisfying the claimed structural limitations**. Ex Parte Masham, 2 USPQ F. 2d 1647 (1987).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
March 17, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER